Analysis of a 170-GHz Frequency Doubler with an Array of Planar Diodes

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Abstract— **Analysis of a planar diode multiplier from 85–170 GHz is described. The doubler uses a waveguide mount with two series pairs of diodes in a balanced structure. Because of the difficulties in conventional scale model measurements, numerical electromagnetic simulation based on the finite element method was chosen for the analysis, using a commercial program. To optimize the diode design, the de-embedded diode terminal impedance was studied, as well as the power balance between the diodes. The analysis showed that the matching of the diode impedance to that of the waveguide is quite sensitive to the diode substrate thickness. Thicknesses from 25–100 μm in GaAs were studied as well as 100-μm-thick quartz. The accuracy of the theoretical analysis was verified by careful measurements using a slotted line to determine the diode terminal impedance under large signal pump, for frequencies between 80 and 90 GHz. Good agreement between the measured and simulated diode terminal impedance was observed, although full agreement requires the addition of an empirical loss term. Several options are considered for the source of this loss.**

I. Introduction

SOLID-STATE local oscillator sources in the THz range are needed for a wide range of applications including laboratory spectroscopy, spaceborne radio astronomy and observations of the earth's atmosphere. One possible way to realize a source for 1 THz would be to start with a Gunn-oscillator at 83 GHz, followed by a frequency doubler, another doubler and finally a tripler. To obtain 0.1 mW output power at 1 THz, the first doubler must have an output power of about 50 mW. This much output power can not be obtained with a single diode, because of the limited power handling, due to both breakdown voltage and saturation effects [1]–[3]. Therefore, an array of diodes is needed. Tests have proved the usefulness of an array of planar diodes in series over a single diode in high power multiplication at 174 GHz [4]. The planar structure with four diodes on a single GaAs substrate has been developed at the University of Virginia [5]. Fig. 1 shows the multiplier and diode that were used in the tests. The diode was designed without the benefit of any modeling. To improve the planar diode design, good modeling of the device is now highly desirable, which must include the interaction of the diode circuit with a waveguide mounting structure. This is particularly important because the manufacturing of a planar diode is a time consuming and expensive process.

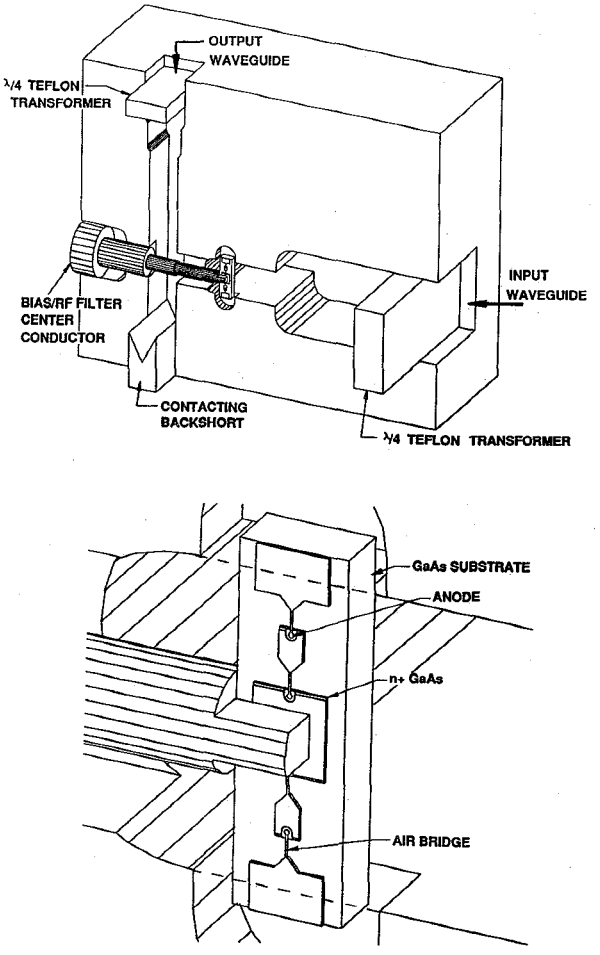

Fig. 1. The planar diode frequency doubler from 85–170 GHz used in the tests and in the finite element analysis. The end pads of the diode are soldered to the mating half of the block.

Conventional scale model measurements, because of the wide range of sizes (>1000:1), are difficult when one considers the smallest important features on the diode relative to the size of a waveguide mount. Another major problem is providing the small coaxial probes to the diode locations. Also, there are mechanical inaccuracies inherent in the fabrication of the model, such as with the attachment of metal tapes, as are often used [6]. We have instead chosen to do numerical electromagnetic simulations on the multiplier. The advantages of numerical analysis are that one may easily study dielectric thickness

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effects, optimum inductances in the diode package, power balance between the diodes, and the origin of the parasitic effects. Other advantages are the provision for multiple probe ports, and the ease with which the structure can be split into pieces and with which parts of the structure can be added or deleted to see their effects. In this paper we describe analyses based on the finite element method which we have carried out on a planar diode doubler from 85–170 GHz. The verification of the accuracy of the finite element analysis (FEA) through input impedance measurements is also described as well as the study of losses in the planar diode structure. Our method of applying the FEA to a multiplier can be easily used for other devices with non-linear properties. The finite element method of analysis is becoming widespread. A study of planar diode parasitic elements by the FEA is described in [7] and a comparison of measured and simulated results of a waveguide to microstrip transition in [8].

II. Approach to the Analysis

In the analysis, the HP85180A High Frequency Structure Simulator program (HFSS) by Hewlett-Packard was used. This program performs FEA on closed arbitrary geometries with lossy and lossless metals and dielectric materials. The HFSS includes only linear analysis, while a varactor diode is a very nonlinear load. The non-linear circuit simulation to determine optimum source and load impedances was done separately using a harmonic-balance analysis program (HP85150B Microwave Design System (MDS) by Hewlett-Packard).

Fig. 1 shows the doubler from 85–170 GHz that was analyzed. In our finite element analysis, the non-linear parts of the doubler were treated in two ways. 1) Small probes were connected to the diode locations in a similar way to that which would be done in scale model measurements. 2) The non-linear Schottky contact was substituted with a linear lossy capacitor, which had a resistance and reactance equivalent to the diode impedance at the frequency of the analysis.

In both cases, the diode impedance was calculated with the harmonic-balance analysis, by finding the optimum input and output embedding impedances under optimum bias conditions. In the electromagnetic analysis, the reduced input and output circuits of the multiplier were used. Fig. 2 shows the reduced and simplified input circuit of the multiplier shown in Fig. 1. Comparison of the results showed that the input backshort can be included either in the finite element analysis or later in the circuit analysis. Because the latter alternative was chosen, the reduced input waveguide circuit is just a simple piece of waveguide with a port in each end. This approach is more flexible from the de-embedding point of view. In the real device the fixed input backshort was 0.41 mm from the diode. The input waveguide TE_{10}-mode does not couple to the TEM-mode in the coaxial line between input and output waveguides. Therefore, the input circuit ends at the fixed curved backshort of the input waveguide. Due to the symmetry, only half of the circuit is needed. The reduced input circuit does not include the waveguide step shown in Fig. 1, which is part of the $\lambda/4$ impedance transformer in the actual doubler.

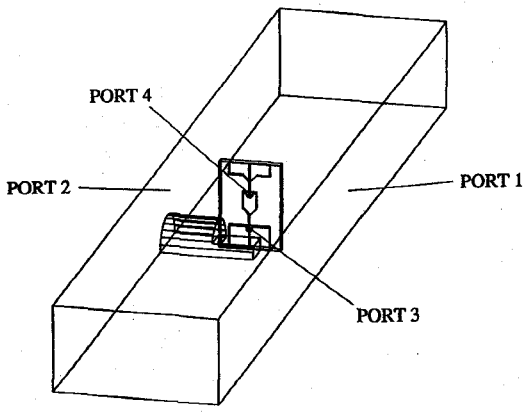

Fig. 2. Reduced and simplified input circuit for the finite element analysis. The actual analysis includes longer waveguide ports (ports 1 and 2) to suppress higher modes.

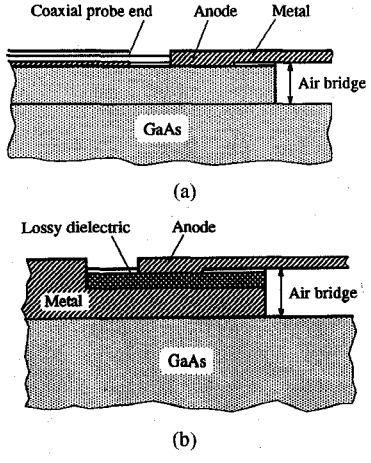

Fig. 3. Cross-sectional view of the diode junction area (a) accessed with a small coaxial probe and (b) modeled as a lossy capacitor.

A. Probe Ports to the Diode Locations

Fig. 3(a) shows the cross-section of a diode location with a small probe. The output of the finite element analysis is a generalized four-port S-matrix. There is one port to each diode location and one port in each end of the input waveguide with the S-parameters of each port normalized to the impedance of the cross section at the port. The four-port S-matrix is combined into an embedding circuit in a circuit simulator, where diode impedances from the harmonic-balance analysis are connected to the diode ports. The de-embedding process, to obtain the diode terminal impedance, includes the addition of waveguides with negative length and correct dispersion and impedance characteristics to the ports. Furthermore, the backshort is substituted with an open circuit. Balance between the absorbed power of the diodes can also be easily calculated from the currents and voltages in the diode ports of the S-matrix.

B. Diodes Modeled as Lossy Capacitor

Instead of leading small probes to the diode locations in the finite element analysis, the correct load impedance may be placed at the diode location with a series RC circuit. In the finite element analysis, the RC circuit is easiest to realize by

using a capacitor with lossy dielectric. The cross-section of the diode location, where a lossy capacitor has been placed is shown in Fig. 3(b). The capacitor thickness is 2 μm, which is about two times the thickness of the n-type epilayer of a real Schottky contact. The heavily doped n^+-substrate, under the epilayer, is modeled as a perfectly conducting metal. Losses in the dielectric of a capacitor can be expressed through a complex dielectric constant

$$\hat{\epsilon}\epsilon_0 = (\epsilon' - j\epsilon'')\epsilon_0 \tag{1}$$

where $\epsilon' = \epsilon_r$ is the real part of relative dielectric constant, ϵ'' is the imaginary part and corresponds to the losses in the material, and ϵ_0 is the dielectric constant of a vacuum. Using (1) and the equation for the capacitance of a plate capacitor, the equivalent series capacitance

$$C_s = C_0 \frac{\epsilon'^2 + \epsilon''^2}{\epsilon'} \tag{2}$$

and resistance

$$r_s = \frac{\epsilon''}{\omega C_0(\epsilon'^2 + \epsilon''^2)} \tag{3}$$

can be derived, where $C_0 = \epsilon_0 A/d$, A is area of the capacitor plates and d is the separation between the plates, and ω is the angular frequency.

The advantage of using lossy capacitors over the small probes is that physically the model corresponds better to a real diode. Due to this, for example, fringing fields around the diode pad can be calculated more accurately. Also, the number of finite elements in the analysis is smaller with a lossy capacitor. This can be an advantage, because the complexity of the analysis is limited by the computer memory resources.

The disadvantage of the lossy capacitor approach is that the analysis relies on the assumption that the frequency dependence of the lossy capacitor impedance is the same as that of the diode, which is true only over a limited bandwidth. Another disadvantage is that the calculation of the division of the absorbed power by each diode junction is not as easy as with the diode probe ports. With lossy capacitors, the power division can be obtained by calculating the pointing vector over a closed surface covering the lossy dielectric.

III. Numerical Considerations

In the case of the HFSS finite element program, 2- and 3-D structures are divided into triangular and tetrahedral sections, respectively. Inputs and outputs to the structure are obtained through ports on the outside surface. In each port the desired number of propagating modes are calculated, based on the cross-section of the port. Usually, the port is designed so that only the lowest order mode is supported at the frequency of the analysis. The waveguide attached to each port should extend far enough from the structure with the same cross-section, so that all the evanescent modes have been attenuated at least 30–40 dB. This typically means that the length of the waveguide should be at least 1–3 times its width. After the mode(s) in the ports are calculated and the mesh generated, the full electromagnetic field pattern inside the structure, resulting from an excitation wave from one port, is computed. The S-parameters are obtained by calculating the coupling of the field inside the structure to the propagating mode(s) of each port.

To save computer resources, the mesh is adaptively refined until the desired accuracy (convergence) for the S-parameters is obtained. In this process, the mesh points are added iteratively so that the size of the tetrahedra are small compared to the length along which the field changes. Usually, for lossless structures, 5–7 adaptive passes were used to obtain $\Delta S = 0.01$ (change of S-parameters compared to the previous adaptive pass). Analysis of the input circuit was carried out from 75–95 GHz, and the mesh was generated in the middle of the band at 85 GHz. Practically no difference was observed in the results when the mesh was generated at 75 or 95 GHz. Convergence and repeatability of the analysis were generally good: starting from a different initial mesh gave the same results.

IV. Measurement Setup

To verify the reliability of the simulated results, careful measurements of the input impedance of the doubler were made. Using the known input waveguide geometry, the de-embedded diode terminal impedance was calculated from the input impedance. The measurements were carried out between 79.7 and 90.6 GHz.

The main problem in measuring the input impedance of a frequency multiplier is that it depends strongly on bias voltage and absorbed input (pump) power. The available input power for testing this doubler with an array of four planar varactors should be at least 100 mW. A commercial vector network analyzer can not supply this much power at frequencies around 85 GHz. Instead, a WR-10 slotted line was used to measure the complex reflection coefficient, which was in turn used with the de-embedding circuit model to obtain the measured diode terminal impedances. Input reflection may greatly reduce the absorbed power, invalidating the "high power" measurement. Therefore, before making the actual impedance measurements, the input match was first optimized with a tuner consisting of a $\lambda_g/4$-thick piece of Teflon properly placed in the input waveguide. The use of this simple matching transformer is convenient because its effect on the circuit can be easily predicted in the de-embedding process to obtain the diode terminal impedances. The output match was improved utilizing the same technique, since mismatch in the output affects the input impedance. In this matching process the output power was maximized and the reflected input power was minimized, with resulting VSWR's <2:1 on both ports.

The input impedance measurement set-up is shown in Fig. 4. At 79.7 GHz, a fixed Gunn oscillator with an output power of 140 mW was used, while at other frequencies, a tunable Gunn oscillator with an output power of 100–120 mW was used. The maximum power with the latter Gunn was obtained around 82 GHz and the minimum at the high end of the measurement band. The Gunn oscillator was followed by an isolator and a slotted line. The input waveguide of the doubler was connected to the other end of the slotted line and the output waveguide was connected to a power meter. The probe port of the slotted line was attached to a calibrated

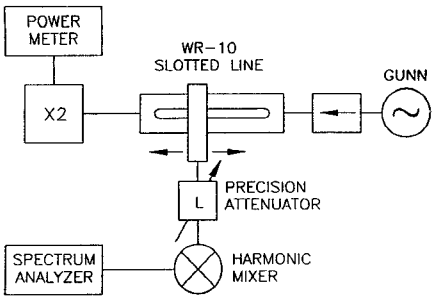

Fig. 4. Setup for measuring the input impedance of the doubler.

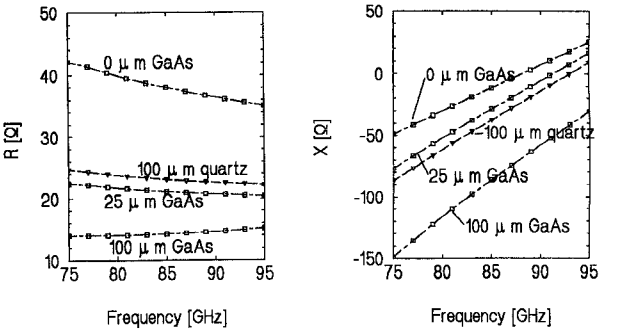

Fig. 5. Real and imaginary parts of the de-embedded diode terminal impedances with 0- , 25- , 100-μm GaAs and 100-μm quartz substrate thicknesses.

adjustable attenuator, which was followed by the harmonic mixer of a spectrum analyzer.

During the measurements, power coupled to the sliding probe was detected with the spectrum analyzer. The actual value of the power ratio was obtained by adjusting the calibrated attenuator. This method of detection is more sensitive than a diode detector and also ensures that the oscillator is at the correct frequency. This was important for accurate measurements, since even a relatively small change in frequency causes a significant error in the location of the standing wave minimum because the probe of the slotted line was more than 15 wavelengths away from the test port. During the measurements the frequency was kept fixed within a few MHz.

Three standing wave minimum locations for both the reference short and the doubler were measured. The differences between the three minimum pairs were calculated and the average of these differences were used to calculate the phase of the reflection coefficient. The magnitude of the coefficient was determined from the average of three power ratios.

V. Results of the Analysis and Comparison with the Measurements

A. Effect of the Thickness of the GaAs Substrate

Experimental tests showed [4] a mismatch between the diode and waveguide mount impedances, with the real part of the diode impedance being lower than that of the mount. Much better matching was obtained by using a thinner GaAs substrate. The original and thinner substrate were about 100 and 25 μm thick, respectively. For the comparison, finite element analyses were carried out for these two cases as well as for the imaginary extreme case of no substrate at all.

Waveguide obstacles and loads such as this diode can be represented as simple shunt elements if their thickness is small enough, but thicker objects require series elements, forming a T-network. In this work, we studied these two possible representations, and found that the simpler two terminal case fits the data very well. In fact, the uncertainties in the values of any additional elements were comparable to their best fit values. Thus we use the two terminal representation in all further discussion. The real and imaginary parts of this impedance are shown in Fig. 5 for various substrates and thicknesses. This data shows that a thinner substrate raises the real part of the impedance, producing a better match to the waveguide in the mount. The variation in the imaginary part indicates a resonance between the diode capacitance and the inductance of the embedding circuit on the chip. We see that the extra capacitance due to the thicker substrate lowers the resonant frequency of the chip, but also increases the Q of this resonance. For best bandwidth, the imaginary part of the impedance should go to zero near the midband of operation, while the Q should be as low as possible. Therefore, the thinner substrate would ideally require more inductance in the package. This argument does not consider the matching at the second harmonic, which may require a lower inductance for the best results.

B. Quartz Versus GaAs Substrate

The need for very thin substrates is driven by the high dielectric constant of GaAs ($\epsilon_r = 12.8$). This has been recognized as one of the major problems with planar diodes, and several workers have successfully replaced the GaAs with a quartz substrate in a multistep process in which the GaAs is etched away and the quartz glued on. While quartz has a lower value of dielectric constant ($\epsilon_r = 3.8$), it is not readily available in thicknesses below 100 μm, although the thickness can be reduced with special handling. In this work, we compared the effect of 25–100 μm thick GaAs with 100-μm-thick quartz, to see if there is a significant benefit to the use of quartz. Fig. 5 shows the de-embedded diode terminal impedance for the cases studied. Comparison of the data shows that 100-μm quartz is slightly superior to 25-μm-thick GaAs, so the process of substrate replacement is really valuable only if the quartz is made thinner than this. The lower thermal conductivity of quartz may be a limitation, however, in this power application.

C. No Air Bridge

Planar diodes are generally designed with an air bridge as a lead to the Schottky contact pads. The air bridge provides a break in the n^+ substrate to avoid a dc short circuit across the diode, a requirement which would otherwise demand a proton isolation of the region. An additional advantage is that air bridges reduce the shunt capacitance over the planar diode junction. However, most of the shunt capacitance is due to the fringing field between the relatively large contact pads through the high dielectric constant GaAs and the finger capacitance

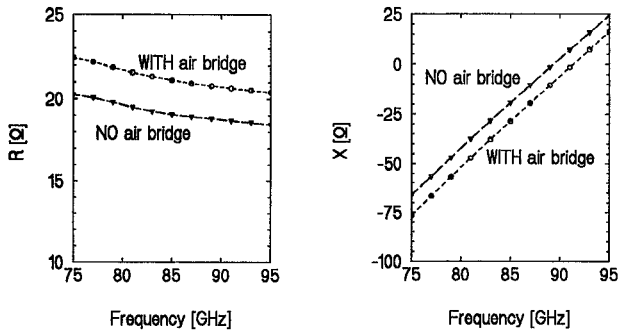

Fig. 6. Real and imaginary parts of the de-embedded diode terminal impedances with and without air bridge (25-μm GaAs substrate).

very close to the anode [9]. To study the electrical advantage of the air bridge geometry, an analysis was carried out with the space under the air bridge filled with GaAs.

Fig. 6 compares the de-embedded diode terminal impedances with and without the air bridge. The substrate is 25 μm thick GaAs in both cases. The comparison shows that electrically the air bridge is only marginally effective with high capacitance varactors ($C_{j0} \approx 40$ fF). For lower capacitance planar diodes, such as those used in mixers, the effect of the air bridge can be more significant. Avoiding the use of an air bridge would improve the handling and mechanical strength of the diode and there would be no mechanical limitations on its length.

D. Power Balance Between the Diodes

To enable efficient use and biasing of all four diodes on the same chip, the absorbed power should be equal for each. For all the structures that were analyzed, the power balance between the diodes (inner diode, which is closer to the bias pin, and outer diode, which is closer to the waveguide wall) was practically frequency independent. However, depending on the structure, the power imbalance varied from 2.7–12.2%. Table I summarizes the power imbalance observed in different cases. The power imbalance is defined here as

$$\Delta P = \frac{P_{\text{outer}} - P_{\text{inner}}}{P_{\text{inner}}}. \tag{4}$$

The values in Table I imply that the environments of the diodes are not symmetric. The primary contribution to the imbalance is the different size of the metallization areas around the diodes. A larger metallization area around the diode junction increases the shunt capacitance and therefore decreases the absorbed power. The addition to the shunt capacitance of the inner diodes due to the large bias pin is less than a few percent, because the fringing fields are concentrated in the high dielectric substrate material.

E. Comparison of Measurements and Simulations

A comparison of the measured and simulated de-embedded diode terminal impedances is shown in Fig. 7. During the measurements the diode bias was fixed at 11 V. The input power varied from 100–140 mW. The GaAs substrate thickness of the diode was measured to be 22 $\pm$ 2 μm. The theoretical curve was calculated using the above input power,

TABLE I
ABSORBED POWER IMBALANCE BETWEEN THE INNER AND OUTER DIODE JUNCTIONS. A POSITIVE PERCENTAGE MEANS THAT THE OUTER DIODE JUNCTIONS ARE ABSORBING MORE POWER THAN THE INNER DIODE JUNCTIONS

Substrate	Power imbalance ΔP
GaAs 0 μm	2.7 %
GaAs 25 μm	8.9 %
GaAs 100 μm	9.2 %
GaAs 25 μm (no air bridge)	12 2 %
GaAs 25 μm (no bias pin)	7.4 %
Quartz 100 μm	3.1 %

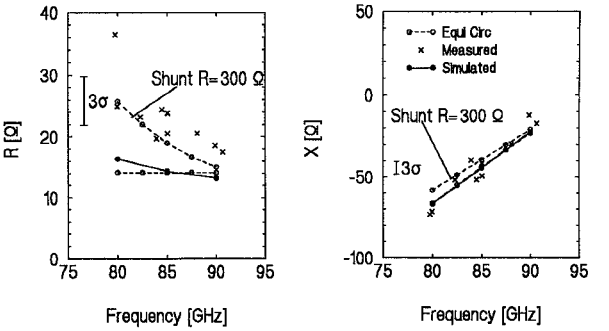

Fig. 7. Real and imaginary parts of the measured and simulated de-embedded diode terminal impedances. The simulated curve is calculated for a 22 μm GaAs thickness using real input power levels and bias voltages for the diode. Also shown are the impedances calculated using the equivalent circuit with and without a 300-Ω shunt resistor.

TABLE II
SOURCES OF ERROR IN THE SLOTTED LINE MEASUREMENT OF THE DIODE TERMINAL IMPEDANCE

Source of error	Value of the error parameter at 3σ deviation	Value of error ($\pm$) Re(Z)/Ω	Im(Z)/Ω
VSWR	Accuracy of power ratio 1 dB	0.3	1.5
Phase of ρ	Δang(ρ) = 30°	2.0	1 25
Losses in WG mount	10 % loss assumed	0.25	0.25
Input power inaccuracy	P reduced from 100 to 40 mW	1.5	2.25
Output mismatch	Trans. moved $\lambda_g/4$ from opt. pos.	2.25	2.25
Input trans. not ideal shape	Real shape simulated with HFSS	-	-
Input trans. tilted	Tilted 102 μm from one end	1.0	1.0
Input trans. position	Position changed 51 μm	1.5	1.25
Input trans. thickness	Thickness changed 51 μm	1.0	1.0
De-embedding frequency	Frequency changed 100 MHz	0.3	0.6
TOTAL ERROR (RSS) 3σ		±4.0	±4.1

bias voltage, and substrate thickness. The second harmonic termination was chosen to be the value for optimum efficiency. The effect of different sources of errors on the measurement is shown in Table II. The overall accuracy (3σ) of the measurements is about $\pm$4.0 and $\pm$4.1 Ω for the real and imaginary parts, respectively. The random errors were small; at a fixed frequency and doubler setting the real and imaginary parts were repeatable to within 1 and 2 Ω, respectively.

Fig. 7 shows that the imaginary part of the impedance agrees very well with the simulations. The measured real part values are much more scattered, and the difference between the measurements and simulations can not be explained by the measurement errors. The good agreement with the imaginary part of the measured and simulated values can be explained by the clear physical origin of the reactance. The reactance is mainly defined by the capacitance of the planar diode, which is due to the fringing fields in the planar structure and the junction capacitance. The origin of the real part of the

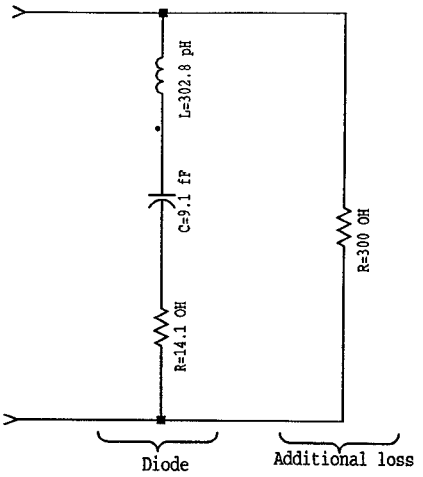

Fig. 8. The equivalent circuit of the planar diode at the input frequency. This circuit includes a shunt resistor, which can explain the measured real part of the diode terminal impedance.

terminal impedance is more complex. In addition to the series resistance of the junction, the termination of the second and third harmonics affects the real part [10]. However, the real part of the varactor impedance is very constrained because it is closely linked to the efficiency of the doubler. Its value can not increase significantly over that at peak efficiency for any choice of harmonic terminations. Harmonics above the second were terminated with opens in this work, which is close to the optimum. The lower limit for the real part of the impedance is the intrinsic series resistance of the diode.

The discrepancy between the measured and simulated real part of the diode terminal impedance implies the presence of a loss in the real doubler circuit that has been missed by the lossless finite element simulations. A simple equivalent circuit of the planar diode is shown in Fig. 8, which includes a shunt resistance simulating the losses in the doubler structure. Comparison of the diode terminal impedance, calculated using this equivalent circuit and the HFSS-MDS simulations, is also shown in Fig. 7. This figure shows that a shunt resistance of 300 Ω could explain the higher measured real parts of the diode terminal impedance, so a further study of losses was made.

VI. Possible Sources of Loss in the Doubler Structure

Four main sources of loss in the doubler structure are likely: 1) waveguide losses, 2) limited conductivity of the n^+ region underneath the metal pads of the planar diode, 3) losses in the GaAs substrate, and 4) losses in the back surface of the planar diode chip (the rough ground surface formed during the thinning of the diode chip). A 10% waveguide loss has been included in the error analysis described earlier. The input waveguide is only 12 mm long, and this loss is already higher than is typically measured for this length. The effect of the limited n^+ region conductivity was studied by the FEA. In the analysis a conductivity of 1000 S/cm was used. No significant change was observed for the real part of the diode terminal impedance.

The results of the FEA for the case of loss in the GaAs are shown in Fig. 9. This figure shows that a value of $\tan\delta = 0.3$

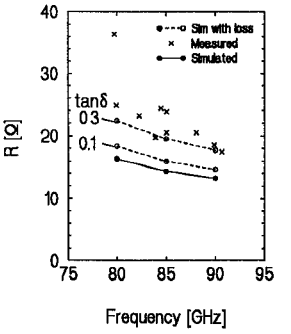

Fig. 9. Real part of the measured and simulated de-embedded diode terminal impedances. The GaAs substrate loss is included in the simulated curves.

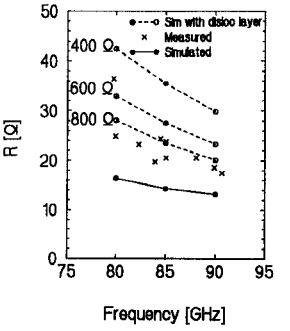

Fig. 10. Real part of the measured and simulated de-embedded diode terminal impedances for the case of a lossy dislocation layer on the back side of the diode (simulated by a resistive layer).

for the GaAs substrate does raise the simulated values closer to the measured ones. However, because this value of $\tan\delta$ is 10–100 times larger than expected and because the slope of the simulated curve of the real part does not seem to agree very well with the measured values, the loss in the GaAs substrate is assumed not to be the main explanation for the loss in the doubler circuit.

Since the above three sources of loss did not seem to be very likely explanations, we finally considered a possible layer of dislocations on the back side of the chip caused by the mechanical thinning process. We assume that the surface states at the many grain boundaries cause this surface to behave like a poor conductor. The dislocation layer was simulated in the FEA by placing an infinitely thin resistive layer on the back side of the diode chip. Fig. 10 shows the results of these simulations. The resistance values for the layer, shown in the figure, are over the full length of the diode. Simulations with a resistive layer of 800 Ω predict very similar real part values to the measurements. While this mechanism is fully consistent with the measured data, no independent data are available to quantify the loss expected in a roughened surface, so we can not conclude how likely this explanation may be. Similar results were obtained by placing a very lossy 4-μm-thick layer on the back side of a 18-μm-thick substrate. The imaginary part of the diode terminal impedance in these simulations did not change significantly compared to the lossless case.

VII. Conclusion

A frequency doubler for 170 GHz having an array of four planar diodes has been analyzed using the finite element

method. The doubler has given excellent results in actual tests, and the work here was aimed at obtaining a better understanding of the diode terminal impedances in the waveguide mount, in order to optimize the diode chip.

The thickness of the substrate was varied in the analysis, which showed that a GaAs thickness less than 25 μm is needed for best matching to the waveguide. If quartz is substituted for the GaAs, equivalent results are obtained for a thickness of about 100 μm. The effect of air bridges in the GaAs diode structure was also studied, and they were found to be only marginally useful in reducing the parasitic capacitance of the diode. A small imbalance was found in the power absorbed by the diodes. The power coupling could be better matched by adjusting the areas of the metal pads surrounding the anodes.

The accuracy of the theoretical analysis was verified by careful measurements of the input impedance of the doubler, which were then used to compute diode terminal impedances. These measurements were performed in the 80–90 GHz range using a slotted line and a high power source. Matching to the doubler was optimized at the input and output with Teflon tuners to ensure that a high pump power actually reached the diodes, and the effect of these tuners was then de-embedded in the following analysis. Good agreement was observed between simulations and experiment in the imaginary part of the diode terminal impedance, but the real part showed some systematic variation. This may be due to unexpected losses within the diode chip, and we studied three possible sources for this loss. The best fit is found for losses in the mechanically rough layer formed in the thinning of the chip.

Overall, the good agreement between the measured and simulated results has convinced us of the value of the finite element method, even in a situation such as this with considerable complexity and a very large range of size scales.

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